REMARKS

Reconsideration of this patent application is respectfully requested in view of the following remarks.

It is noted that the Patent Examiner has repeated, and made Final, the previous Requirement for Restriction.

The Patent Examiner has rejected Claims 13 - 15 under 35 U.S.C. 103 (a) as being unpatentable over *Wijaranakula et al. U.S. Patent No. 6,022,793* in view of *Graef et al. U.S. Patent No. 5,935,320.*

Wijaranakula in column 3 in lines 8-25 discloses a method of creating gettering sites in an epitaxial wafer, the method comprising

implanting silicon ions into a substrate of the wafer;

implanting oxygen ions into the substrate of the wafer;

thermally annealing the substrate of the wafer for a period of time sufficient to nucleate defects in the substrate; and

depositing an epitaxial layer upon a surface of the substrate, thereby forming gettering sites from the nucleated

defects in the wafer.

Thus, there is a semiconductive wafer comprising a substrate and an epitaxial layer on the substrate, wherein the substrate contains dislocation loops as gettering sites anchored by oxygen precipitate clusters so as to prevent the dislocation loops from sliding to the surface of the wafer over time.

Wijaranakula in column 6 in lines 7 to 18 discloses that the thickness of the epitaxial layer may be, for example, from less than 1μm up to about 100μm, preferably from less than 1 μm up to 15μm. The epitaxial layer, like the substrate, may be doped with any suitable dopant including, for example, boron, phosphorous, antimony, arsenic and the like. The dopant concentrations may be similar to those for the substrate discussed above, although the epitaxial layer may contain a lower concentration of dopant than the substrate. The epitaxial layer may also have a specific resistivity similar to that of the substrate, for example ranging from about 5 mΩcm to about 50 Ωcm, preferably 0.1 to 15 Ωcm.

However, *Wijaranakula* fails to disclose doping with nitrogen or providing an epitaxial layer having a surface on which fewer than 30 LLS defects with a size of more than 0.085 µm can be detected.

Graef in column 2 in lines 40 to 50 discloses a process for producing silicon wafers with low defect density, comprising the steps of:

a) preparing a silicon single crystal having an oxygen doping concentration of at least $4*10^{17}/cm^3$ and a nitrogen doping concentration of at least $1*10^{14}/cm^3$;

b) processing the silicon single crystal to form silicon wafers; and

c) annealing the silicon wafers at a temperature of at least 1000°C. For at least one hour.

However, *Graef* fails to disclose an epitaxial layer with fewer than 30 LLS defects with a size of more than 0.085µm.

The Patent Examiner has contended on page 3 of the Office Action that the modified *Wijaranakula* et

al.semiconductor wafer has the same structure as claimed. Thus, it was alleged to be inherent that the epitaxial layer has a surface on which fewer than 30 LLS defects with a size of more than 0.085 µm can be detected. This contention is respectfully traversed.

Neither of these prior art references recognize the problem solved by the present invention. This is discussed on Page 1 of the present Specification.

At the present time intensive investigations are under way with the aim of establishing which features semiconductor wafers with an epitaxial layer have to have in order to qualify them as a base material for the production of modern CMOS components. According to the publication in Jpn. J. Appl. Phys. Vol. 36 (1997), pp. 2565-2570, a semiconductor wafer comprising a p-doped substrate wafer and a likewise p-doped epitaxial layer having a thickness of 1µm is particularly suitable for large scale integrated CMOS applications. This appraisal is also supported by the publication in Electrochemical Society Proceedings Volume 98-1, pp. 855-861. However, this paper also draws attention to light-scattering defects (light point defects) on the surface

which occur in a semiconductor wafer with a thin epitaxial layer but do not adversely affect the GOI (gate oxide integrity). The above mentioned defects are called LLSs (localized light scatters) by experts. Despite their indifferent behavior with regard to the GOI, the LLSs are undesirable to manufacturers of integrated circuits, which is also demonstrated by the fact that the ITRS (International Roadmap For Semiconductors) demands that the number of LLS with a size of greater than or equal to 0.085 μm be less than or equal to 38 per semiconductor wafer with an epitaxial layer. This requirement applies to 0.18 μm technology and it must be assumed that as miniaturization advances (0.13 μm and below), an even more stringent requirement will be imposed on the number of LLSs. Moreover, the limit value of 38 LLSs represents a maximum value and it should be taken into account that the number required for an industrial process capability must be significantly less than that.

Nowhere in the prior art is there a teaching or a suggestion as to the solution to this problem, which solution is provided accorded to the present invention.

Thus, an object of the present invention is to provide a semiconductor wafer with an epitaxial layer which is suitable for modern CMOS applications, has a particularly small number of LLSs and requires comparatively low production costs. The object of the invention is, moreover, to specify a process for producing the semiconductor wafer.

The present invention relates to a semiconductor wafer, comprising a substrate wafer made of monocrystalline silicon and an epitaxial layer deposited thereon, which is characterized in that the substrate wafer has a resistivity of from 0.1 to 50 Ωcm, an oxygen concentration of less than $7.5*10^{17}$ $atcm^{-3}$ and a nitrogen concentration of from $1*10^{13}$ to $5*10^{15}$ $atcm^{-3}$, and the epitaxial layer has a thickness of from 0.2 to 1.0 μm and has a surface on which fewer than 30 LLS defects with a size of more than 0.085 μm can be detected.

The Patent Examiner argues that it would be obvious to a person having ordinary skill in the art at the time the invention was made to form the substrate wafer of *Wijaranakula et al* having an oxygen concentration of $4.5*10^{17}$ $atcm^{-3}$ and a nitrogen concentration of $2.5*10^{14}$ $atcm^{-3}$ using the process taught by *Graef et al* in order to provide silicon

wafers with a low defect density after annealing.

In response thereto, the present invention is not merely a substrate wafer, but instead is a substrate wafer having an epitaxial layer deposited on its surface. If the Examiner's argument is accepted, then a person having ordinary skill in the art would have also treated the substrate wafer taught by *Graef et al* in accordance with the process taught by *Wijaranakula et al.* This is because *Graef et al* do not disclose any further processing of the substrate wafer to achieve an epitaxial wafer. Accordingly, the substrate wafer taught by *Graef et al* would have been subjected to the process taught by *Wijaranakula et al* in order to produce an epitaxial wafer with gettering sites in the bulk for capturing impurities. However, this process includes an ion implantation step with oxygen ions being implanted into the substrate wafer in order to generate the intrinsic gettering sites. The implantation of additional oxygen leads to a local increase of the oxygen concentration near the surface of the substrate wafer. The peak concentration of oxygen is much greater than the $7.5 * 10^{17}$ limit of claim 13 as shown in FIG. 2. of *Wijaranakula* of which shows greater than 10^{19} for oxygen concentration.

Hence, the combination of *US-6,022,793* and *US-5,935,320* leads to an epitaxial wafer having at least locally an oxygen concentration which is higher than $7.5*10^{17}$ $atcm^{-3}$ which is the limit concentration claimed in the present patent application. Accordingly, the claimed wafer has a structure which is very different from the prior art. Moreover the prior art wafer is additionally subject to an ion bombardment, which causes further significant structural differences.

Thus the Patent Examiner's argument is respectfully traversed that the prior art epitaxial wafer inherently has a surface on which fewer than 30 LLS defects with a size of more than 0.085 µm can be detected. This is because the prior art processes would produce an entirely different wafer from that being claimed.

In conclusion, none of the prior art references, whether considered singly or in any combination, teach or suggest the present invention under 35 U.S.C. 103. Withdrawal of this ground of rejection is respectfully requested. A prompt notification of allowability is respectfully requested.

Respectfully submitted,

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